AMENDMENTS TO THE SPECIFICATION

Please add the following new paragraph after paragraph **[0045]**:

Figure 9 illustrates switches used to set or configure timers, Figure 10 illustrates examples of clock periods using some of the switches in Figure 9, and Figures 11-13 illustrate other example setting of the switches illustrated in Figure 9.

Please replace paragraph **[0108]** with the following amended paragraph:

Figures 9-13 illustrate Tables 6-9, and 11. In Figures 9-13, The switches labeled "CommDIP1-7" form the input to a 7-bit binary counter, CommDIP1 being the "least significant bit" and CommDIP7 being the "most significant bit". The timer counts up to the value specified on the CommDIP switches before resetting to create the variable delay required. The switches labeled CommDIV0-1 are used to dictate the input clock speed into the timer. Table 7 below shows all available clock periods assuming 10 MHz clock is used to clock the FPGA controller.